ABSTRACT OF THE DISCLOSURE

A computer system includes an integrated core and graphic controller device having a core logic controller portion and a graphic controller portion, a system memory pool, and a stand-alone frame buffer memory pool separate from the system memory pool. A first memory data bus interconnects the integrated core and graphic controller device and the system memory pool. A second memory data bus interconnects the integrated core and graphic controller device and the frame buffer memory pool. A memory address and control signal bus interconnects the integrated core and graphic controller device, the system memory pool and the frame buffer memory pool. The graphic controller portion of the integrated core and graphic controller device generates a same set of address signals received by the system memory pool and the frame buffer memory pool via the memory address and control signal bus such that the graphic controller portion is able to access simultaneously first word part display data from the system memory pool via the first memory data bus and second word part display data from the frame buffer memory pool via the second memory data bus.